REMARKS

Applicants respectfully request reconsideration of this application as amended. Applicants submit the following response to overcome the Examiner's rejection. Claims 63-90 are still pending.

Rejections Under 35 U.S.C. § 102(e)

In the Office Action, the Examiner has rejected claims 63-75 and 77-89 under 35 U.S.C. § 102(e) as being anticipated by Son (U.S. Patent 6,063,681). Applicants respectfully traverse the rejections with the submission of the present amendment.

Applicants respectfully submit that Son fails to teach or suggest the embodiments of the invention of claim 63 claiming a gate electrode having a barrier layer formed on a sidewall of the gate electrode to prohibit the silicidation of the sidewall and claiming a second silicide layer formed after removing a portion of the barrier layer formed over a top surface of the gate electrode.

Applicants respectfully submit that Son fails to teach or suggest the embodiments of the invention of claims 77 claiming a gate electrode having a barrier layer formed on a sidewall of the gate electrode to prohibit the silicidation of the sidewall and claiming second and third silicide layers formed after removing a portion of the barrier layer formed over the top surface of the gate electrode.

Applicants respectfully submit that Son fails to teach or suggest the embodiments of the invention as claimed in independent claims 63 and 77. Accordingly, Applicants respectfully request the withdrawal of the 35 U.S.C. § 102(e) rejections with respect to Son.

Rejections Under 35 U.S.C. § 103(a)

In the Office Action, the Examiner rejected claims 76 and 90 under 35 U.S.C. § 103(a) as being unpatentable over Son (U.S. Patent 6,063,681). Applicants respectfully traverse the rejections with the submission of the present amendment.

Applicants respectfully submit that the amendments to independent claims 63 and 77 overcome the rejections of claims 76 and 90 for the reasons stated above in reference to the Son patent. Accordingly, Applicants respectfully request the withdrawal of the 35 U.S.C. § 103(a) rejections with respect to claims 76 and 90.

Conclusion

In view of the foregoing amendments and remarks, Applicants respectfully submit that all rejections as applied to the claims as amended herein have been overcome and consequently that all claims as they currently stand are in condition for allowance. Applicants respectfully request that all rejections be withdrawn and that the claims be allowed to issue.

Accordingly, Applicants respectfully submit that claims 63-90 are in condition for allowance and Applicants respectfully request the allowance of these claims.

Please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

12-17-02
Date:

William W. Kidd
William W. Kidd
Reg. No. 31,772

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(512) 330-0844

VERSION WITH MARKINGS TO SHOW CHANGES MADE

63. (Amended) A microelectronic structure comprising:

a substrate;

a gate electrode formed over the substrate and defining an underlying channel region in the substrate, said gate electrode having a barrier layer formed on a sidewall of the gate electrode to prohibit the silicidation of the sidewall;

a source/drain extension formed in the substrate adjacent the gate electrode and having a first silicide layer formed therein; and

a source/drain region formed in the substrate adjacent the [gate electrode] source/drain extension and having an activated doped region with a [first] second silicide layer disposed therein [and wherein] , the activated doped region and the [first] second silicide layer are aligned with a spacer disposed along sidewalls of the gate electrode [; and] , said second silicide layer formed after removing a portion of said barrier layer formed over a top surface of the gate electrode, [the] said source/drain [also having an] extension [of the activated doped region wherein the extension has] having less dopant concentration than the activated doped region, and the source/drain extension and [a second] the first silicide layer [disposed in the extension] are aligned with the gate electrode to have the less dopant concentration of the extension reside between the channel region and the activated doped region.

64. (Amended) The microelectronic structure of claim 63, wherein the activated doped region is thicker than the source/drain extension.

65. (Amended) The microelectronic structure of claim 63, wherein the [first] <u>second</u> silicide layer is thicker than the [second] <u>first</u> silicide layer.

66. (Amended) The microelectronic structure of claim 63, wherein the activated doped region and the <u>source/drain</u> extension comprise ion implanted material.

71. (Amended) The microelectronic structure of claim 63, wherein the [first] <u>second</u> silicide layer comprises nickel silicide.

74. (Amended) The microelectronic structure of claim 63, [further comprising a barrier layer adjacent the gate electrode] <u>wherein the gate electrode having a third silicide layer formed on the top surface of the gate electrode</u>.

75. (Amended) The microelectronic structure of claim [74] <u>63</u>, wherein the barrier layer comprises silicon nitride.

76. (Amended) The microelectronic structure of claim 63, wherein the <u>source/drain</u> extension is approximately 300-500 angstroms in thickness.

77. (Amended) A source, drain and gate structure comprising:

a semiconductor substrate;

a gate electrode formed over the substrate semiconductor and defining an underlying channel region in the substrate, said gate electrode having a barrier layer formed on a sidewall of the gate electrode to prohibit the silicidation of the sidewall;

a source/drain extension formed in the substrate adjacent the gate electrode and having a first silicide layer formed therein; and

a source/drain region formed in the substrate adjacent the [gate electrode] source/drain extension and having an activated doped region with a [first] second silicide layer disposed therein [and wherein] , the activated doped region and the [first] second silicide layer are aligned with a spacer disposed along sidewalls of the gate electrode [; and] , said gate electrode having a third silicide layer formed on a top surface of the gate electrode, said second and third silicide layers formed after removing a portion of said barrier layer formed over the top surface of the gate electrode, [the] said source/drain [also having an] extension [of the activated doped region wherein the extension has] having less dopant concentration than the activated doped region, and the source/drain extension and [a second] the first silicide layer [disposed in the extension] are aligned with the gate electrode to have the less dopant concentration of the extension reside between the channel region and the activated doped region.

78. (Amended) The microelectronic structure of claim 77, wherein the activated doped region is thicker than the source/drain extension.

79. (Amended) The microelectronic structure of claim 77, wherein the [first] second silicide layer is thicker than the first silicide layer.

80. (Amended) The microelectronic structure of claim 77, wherein the activated doped region and the source/drain extension comprise ion implanted material.

85. (Amended) The microelectronic structure of claim 77, wherein the [first] second silicide layer comprises nickel silicide.

88. (Amended) The microelectronic structure of claim 77, [further comprising a barrier layer adjacent the gate electrode] wherein the second and third silicide layers comprise a same metal.

89. (Amended) The microelectronic structure of claim [88] 77, wherein the barrier layer comprises silicon nitride.

90. (Amended) The microelectronic structure of claim 77, wherein the source/drain extension is approximately 300-500 angstroms in thickness.